WHAT IS CLAIMED IS:

1. A pulse signal generating circuit for generating a specific pulse signal from a clock signal having a fixed cycle, comprising:

an edge detector configured to detect rising and trailing edges of the clock signal;

a first delay signal generator, including at least one first delay circuit having a first delay value, the first delay signal generator being configured to generate at least one first delay signal whose first delayed edge is delayed by the first delay value in relation to the rising edge of the clock signal;

a second delay signal generator including at least one second delay circuit having a second delay value, the second delay signal generator being configured to generate at least one second delay signal whose second delayed edge is delayed by the second delay value in relation to the trailing edge of the clock signal; and

a logic unit configured to generate a pulse signal by performing logic operations on the first and second delay signals.

2. A pulse signal generating circuit as defined in Claim 1, wherein a cycle duration of the pulse signal is set equal to a cycle duration of the clock signal.

3. A pulse signal generating circuit as defined in Claim 1, wherein the first and second delay values are each set less than half a cycle duration of the clock signal.

4. A pulse signal generating circuit as defined in Claim 1, the first and second delay values are equal to each other.

5. A pulse signal generating circuit as defined in Claim 1, wherein

the edge detector comprises:

a first D flip-flop having a first clock input terminal, a first D input terminal, a first non-inverted output terminal, and a first inverted output terminal, the clock signal being supplied to the first clock input terminal, an inverted output from the first inverted output terminal being fed back to the first D input terminal; and

a second flip-flop having a second clock input terminal, a second D input terminal, a second non-inverted output terminal, and a second inverted output terminal, an inverted signal of the clock signal being supplied to the second clock input terminal, an output from the first non-inverted output terminal of the first D flip-flop being supplied to the second D input terminal,

wherein an output from the first output terminal of the first D flip-flop is supplied to the first delay circuit, and an output from the second output terminal of the second D flip-flop is supplied to the second delay circuit.

6. A method for generating a specific pulse signal from a clock signal having a fixed cycle, comprising the steps of:

(a) detecting rising and trailing edges of the clock signal;

(b) generate at least one first delay signal whose first delayed edge is delayed by a first delay value in relation to the rising edge of the clock signal;

(c) generating at least one second delay signal whose second delayed edge is delayed by a second delay value in relation to the trailing edge of the clock signal; and

(d) generating a pulse signal by performing logic operations on the first and second delay signals.

7. A method as defined in Claim 6, wherein a cycle duration of the pulse signal is set equal to a cycle duration of the clock signal.

8. A method as defined in Claim 6, wherein the first and second delay values are each set less than half a cycle duration of the clock signal.

9. A method as defined in Claim 6, the first and second delay values are equal to each other.